In the Specification:

Please replace paragraph [0012] with the following amended paragraph:

[0012] Inputs from the antennas ~~201A~~ 101A and ~~201B~~ 101B are stabilized at the respective AGC circuits 102 and 104. The output of the AGC circuits 102 and 104 are coupled to the joint timing recovery circuit 200 described with reference to FIG. 2. A common timing signal is derived in the circuit 200 and coupled to the matched filters 106 and 108. The matched filters ~~206~~ 106 and ~~208~~ 108, the FFEs ~~210~~ 110 and ~~212~~ 112, the summer ~~214~~ 114, and the DFE ~~218~~ 118 form a diversity equalizer 150. The matched filters 106 and 108 correlate the input signals in a conventional manner. The FFEs 110 and 112 equalize the matched filter outputs that are then coupled to the summer 114 with the output of the DFE 118. The summed output from the summer 114 is then used in the carrier recovery circuit 116. The carrier recovery circuit 116 recovers the carrier used to transmit the signal to the antennas 101A and 101B. The recovered carrier is then coupled to a forward error correction (FEC) module for further processing.